circuit receiving the first and second reference currents when the current driving circuit does not receive the first and second reference currents responsive to the first and second select signals from the first and second phase detector circuits.

16. The phase detector according to claim 5 wherein the charge pump comprises an integrator circuit.

17. A packetized dynamic random access memory, comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address responsive to a command word;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to the command word;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to the command word; and

a command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a master clock signal, the clock generator circuit comprising:

a first delay-lock loop having a first voltage controlled delay circuit receiving a reference clock signal and generating a sequence of clock signals which are increasingly delayed from the reference clock signal to a last clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal, and a first phase detector comparing the phase of a first and second clock signal in the sequence and generating the first

control signal as a function of the phase difference therebetween, the first phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the first and second clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second edge of the first and second clock signals in the sequence;

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and

a capacitor coupled to the output terminal of the charge pump;

a second delay-lock loop having a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having delay relative to the master clock signal that is a function of a second control signal, and a second phase detector comparing the phase of the master clock signal to the phase of a selected one of the clock signals in the

sequence and generating the second control signal as a function of the difference therebetween, the second phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the master clock signal and the selected one of the clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to received a master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the second phase detector circuit producing a second select signal having a duty cycle according to the phase relationship between a second edge of the master clock signal and the selected one of the clock signals in the sequence; an

a charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, an increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and

a capacitor coupled to the output terminal of the charge pump;

a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the

multiplexer as a function of a select signal applied to a control input of the multiplexer; and

a select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit to store the command data packet and generating the select signal corresponding thereto.

18. The packetized dynamic random access memory of claim 17 wherein the first combination of logic levels is the first and second select signals at different logic levels, the second combination of logic levels is the first and second select signals at a high logic level, and the third combination of logic levels is the first and second select signals at a low logic level.

19. The packetized dynamic random access memory of claim 17 wherein the first and second phase detector circuits comprise:

a first signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the first signal transition detector producing a first trigger pulse signal in response to the respective input clock signal changing logic states;

a second signal transition detector having an input terminal coupled to receive a respective input clock signal and an output terminal, the second signal transition detector producing a second trigger pulse signal in response to the respective input clock signal changing logic states; and

a flip-flop having first and second input terminals coupled to the output terminal of the first transition detector and the output terminal of the second transition detector, respectively, and first and second output terminals coupled to a respective input terminal of the charge pump, the flip-flop set responsive to the first trigger pulse signal and reset responsive to the second trigger pulse signal.

20. The packetized dynamic random access memory of claim 17 wherein the charge pump comprises:

a first current generator circuit coupled to a first reference voltage;

a second current generator circuit coupled to a second reference voltage; and

a charging circuit coupled between the first and second current generator circuits and having first and second input terminals coupled to a respective output terminal of the first and second phase detector circuits, and an output terminal coupled to transmit the control signal to the output terminal of the charge pump.

21. The packetized dynamic random access memory of claim 18 wherein the first and second current generator circuits are current mirror circuits.

22. The packetized dynamic random access memory of claim 17 wherein the charge pump is an integrator circuit.

23. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory coupled to the processor bus adapted to allow data to be stored, the dynamic random access memory comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address responsive to a command word;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to the command word;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to the command word; and

a command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a master clock signal, the clock generator circuit comprising:

a first delay-lock loop having a first voltage controlled delay circuit receiving a reference clock signal and generating a sequence of clock signals which are increasingly delayed from the reference clock signal to a last clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal, and a first phase detector comparing the phase of a first and second clock signal in the sequence and generating the first control signal as a function of the phase difference therebetween, the first phase detector comprising:

a first phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the first phase detector circuit producing a first select signal having a duty cycle according to the phase relationship between a first edge of the first and second clock signals in the sequence;

a second phase detector circuit having first and second input terminals coupled to receive the first and second